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HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS.(U)
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SEVENTH QUARTERLY DEVELOPMENT REPORT

FOR

HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS

3 AUGUST 1977 TO 3 NOVEMBER 1977

Prepared By
RCA Solid State Divison
Route 202, Somerville, N.J. 08876

For

DEPARTMENT OF THE NAVY
NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.

Contract No. N00039-76-C-0240
Project No. 62762N
Subproject No. XF54586
Task No. 002

SEVENTH QUARTERLY DEVELOPMENT REPORT

FOR

(6) HIGH-RELIABILITY, LOW-COST INTEGRATED CIRCUITS

(9) Quarterly development rept. no. 7,
3 AUG [redacted] 3 NOV [redacted] 77.

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RCA Solid State Divison
Route 202, Somerville, N.J. 08876

(11) 3 Nov 77
(12) 35 P.

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SECTION I

ABSTRACT

Wafer fabrication is nearly completed. COS/MOS circuits have been successfully fabricated utilizing sputter etch technology for platinum definition.

Trimetallization technology with silicon nitride overcoat passivation, copper beam-tape automated assembly, and silicone molding compound has proven to be the best system for fabrication of high reliability low cost integrated circuits.

SECTION II
PURPOSE

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high reliability integrated circuits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve semiconductor reliability which will meet military requirements without a severe cost penalty.

The approach to achievement of the goals of this program is the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. The program is being carried out in three phases.

Phase I - Completed

(a) Process Feasibility - The required photomasks were generated using existing masks to the maximum extent possible. Then, small quantities of each device type were fabricated to assure that the masks and processes were available for the production runs of Phase II. Also, each device type was fabricated using a matrix of carefully varied process parameters to assess their impact on yields and reliability.

(b) Process Development - The processes required to fabricate the eight integrated-circuit types to be produced in Phase II were defined and documented. Silicon nitride passivation and the titanium-platinum-gold metallization system were used to achieve chip hermeticity and a corrosion-free metallization system. In addition, a silicon nitride overcoat layer was applied for protection of the metallization. A series of experiments was completed at each critical processing step to

assure repeatability. Real-time indicators and accelerated life tests were used to assess the effects of process changes on reliability and to measure progress in achieving the required failure rate.

(c) Automated Assembly - The technology being used in Phase II was defined and documented. The effect of assembly process parameters on cost and yield was assessed. Bonding tapes and lead-frames compatible with each of the device types were designed and fabricated. A number of devices of each type were assembled using the automated assembly system. Reliability was monitored continually by means of accelerated life tests.

The photomasks, wafer process, and assembly process required to fabricate the eight integrated-circuit types in the low-cost high-reliability device-fabrication phase have been defined and documented and sample devices of each type were fabricated. Additionally, preliminary reliability data have been generated to demonstrate the soundness of the chosen approach.

At this time, the production runs of Phase II have begun.

Phase II - Fabrication

The low-cost high-reliability device fabrication phase of the program involves significant quantities of each of the eight selected integrated-circuit types fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits are being constructed in both plastic and ceramic packages. This will permit a detailed comparison to be made of the new and conventional processes. During these production runs, any significant differences between the two processes are being defined and documented. The utilization of existing equipment and mask sets is being demonstrated, and the cost impact of converting to this type of processing will be estimated. In-process quality controls, real-time indicators, and parameter distributions

at wafer probe and final test are being used to monitor the production run and to assure process reproducibility. All devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and asembled.

Phase III - Reliability

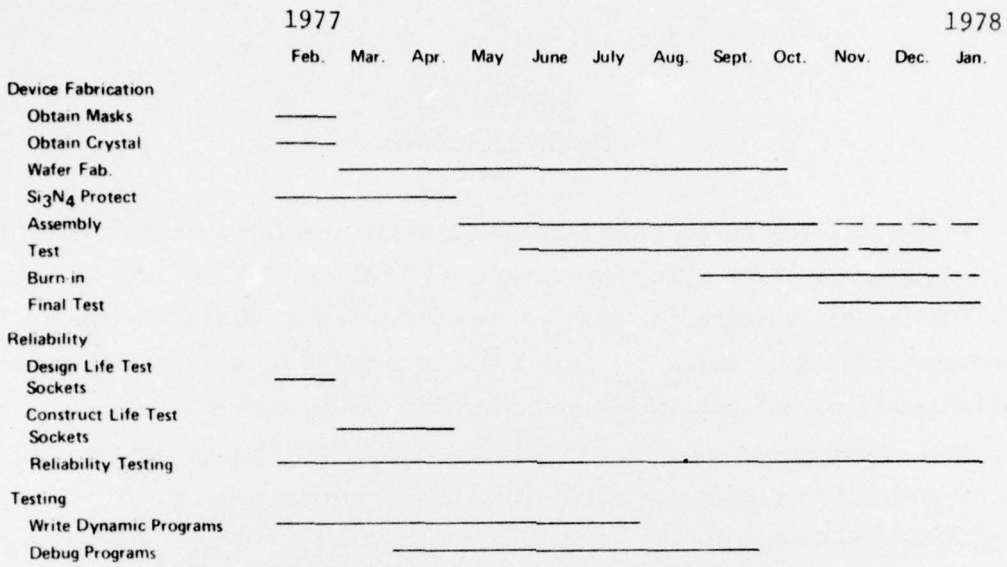
The reliability of the devices produced in Phase II will be demonstrated. The conventional aluminum-metallized integrated circuits, packaged and tested to military high-reliability requirements, will be used as the baseline from which to appraise the new process developed under the program. In addition, the level of testing required over and above commercial screening to assure a reliable product for military end use will be determined, and the cost impact of this testing will be analyzed and verified.

SECTION III
PHASE II PROGRAM

Phase II, the low-cost high-reliability device-fabrication phase of the program, involves significant quantities of each of the eight selected integrated-circuit types to be fabricated according to the processes defined in Phase I. Both silicon nitride passivated, titanium-platinum-gold metallized integrated circuits and conventional silicon dioxide, aluminum-metallized integrated circuits are being constructed in both plastic and ceramic packages. This plan permits a detailed comparison to be made of the new and conventional processes. During these production runs, significant differences between the two processes are being defined and documented. The utilization of existing equipment and mask sets is being demonstrated, and the cost impact of converting to this type of processing is being estimated. In-process quality controls, real-time indicators, and parameter distributions at wafer probe and final test are being used to monitor the production run and to assure process reproducibility. Devices produced in this phase of the program will be utilized in Phase III for reliability testing and delivery to the Navy. Finally, the testing facilities for the Phase III program will be defined and assembled. The milestone chart for Phase II is shown in Fig. III-1.

As shown in Fig. III-2, the minimum quantity of units required for delivery to the Navy and for the Phase III test plan is 5165 devices per type. Reliability testing during Phase II will require additional units, and other needs will surface during the course of the contract. It is anticipated, therefore, that approximately 10,000 units of each type will be fabricated during Phase II.

In addition to initiating the long-term 125°C life tests during Phase II, a program of accelerated life testing is planned for two circuits,



Dashed line indicates revised schedule.

Fig. III-1 - Phase II Milestone Chart

Type	CD4012B	CD4014A	CD4027B	CA741	5420	54S20	5470	5472
Technology	COS/MOS	COS/MOS	COS/MOS	Bipolar Linear	Au-T^2L	Schottky	Au-T^2L	Au-T^2L
Wafer Lot Size	25	25	25	25	25	25	25	25
Net Units Required								
Internal								
Al DIP	115	→						
Al DIC	145	→						
Trimetal DIC	155	→						
Trimetal DIC (Unencapsul.)	25	→						
Trimetal DIP	725	→						
To Be Delivered	4000	→						
Total	5165	→						

Fig. III-2 - Phase II Device Fabrication Plan.

the CA741 and the CD4012B. This program will verify the reliability goals, compare encapsulation techniques, compare the results achieved with devices in dual-in-line ceramic packages, and establish the activation energy to be used for extrapolating the results of accelerated tests. The planned test matrices are shown in Fig. III-3.

Life Tests	Encapsulation Technique				
	Silicone	Epoxy Novolac	Epoxy Novolac With Junction Coat	DIC	Non-Hermetic DIC
Bias					
150°C	20	20	20	15	15
175°C	20	20	20	15	15
200°C	20	20	20	15	15
225°C	20	20	20	15	15
250°C	20	20	20	15	15
Storage					
150°C	15	15	15	10	10
175°C	15	15	15	10	10
200°C	15	15	15	10	10
225°C	15	15	15	10	10
250°C	15	15	15	10	10
Step Stress					
150°C	20	20	20	15	15

Types: CD4012B, CA741

Fig. III-3 - Phase II Test Plan.

SECTION IV

DETAILED FACTUAL DATA

TECHNICAL DISCUSSION

Product Generation

Processing of all integrated circuit wafers will be completed by December 31. Assembly has been delayed pending accumulation of data from the step-stress tests. The status of the eight integrated circuit types is shown in Fig. IV-1. Sputter etching of the COSMOS circuits for platinum definition has proven to be a useful technology for closely spaced metal lines.

Reliability Testing

Copper Migration

After 4000 hours of testing at T_j = 155°C, 4/37 devices failed due to copper dissolution and redeposition in the epoxy molding compound. This precludes the use of epoxy novolac molding compound with copper beam tapes. The reliability of the silicone molding compound has been excellent with respect to temperature, electrical parameters, sequential salt atmosphere and moisture testing. The Phase II final samples will be assembled using the silicone molding compound.

Status of Life Test Sockets

All of the necessary life test sockets for Phase II of the program have been received with the exception of the 250°C bias life sockets for 4012B. These were not satisfactory as received and will be corrected.

Sequence Test Summary

The summary of results to date for sequential testing of CA741G devices with silicon nitride dielectric overcoating and silicone molding compound is updated in Fig. IV-2.

	TA NO.	DESCRIPTION	ALUMINUM	TRIMETAL
1.	TA10151	5420 DUAL 4-INPUT NAND GATES	READY FOR ASSEMBLY	AT CIRCUIT PROBE
2.	TA10152	54S20 SCHOTTKY DUAL 4-INPUT NAND GATE	READY FOR ASSEMBLY	AT Si_3N_4 OVERCOAT
3.	TA10153	5470 EDGE-TRIGGERED J-K FLIP-FLOP	READY FOR ASSEMBLY	AT Si_3N_4 OVERCOAT
4.	TA10154	5472 MASTER SLAVE J-K FLIP-FLOP	READY FOR ASSEMBLY	AT Si_3N_4 OVERCOAT
5.	TA10155	CD4012B COS/MOS DUAL 4-INPUT NAND GATE	READY FOR ASSEMBLY	1/3 READY FOR ASSEMBLY 1/3 AT Si_3N_4 OVERCOAT 1/3 AT SPUTTER ETCH
6.	TA10156	CD4027B COS/MOS DUAL J-K FLIP-FLOP	AT CIRCUIT PROBE	1/3 AT CIRCUIT PROBE 1/3 AT Si_3N_4 OVERCOAT 1/3 AT SPUTTER ETCH
7.	TA10219	CD4014A COS/MOS 8-STAGE SHIFT REGISTER	AT CIRCUIT PROBE	1/3 AT CIRCUIT PROBE 1/3 AT Si_3N_4 OVERCOAT 1/3 AT SPUTTER ETCH
8.	TA10158	CA741 OPERATIONAL AMPLIFIER	AT CKT PROBE	AT GOLD BUMPING

Fig. IV-1 - Wafer fabrication status.

SEQUENCE TEST SUMMARY

TYPE	PROTECTIVE LAYER	ASSEMBLY	MOLDING COMPOUND	TEST	RESULTS
CA741G	PSG	WIRE BOND	SILICONE	96 Hours Salt Atmosphere (Method 1009.1)	0/10
				plus	
				336 Hours 85°c/85% RH Bias Life	3/10
				TEST COMPLETE	
CA741G	PLASMA Si_3N_4	BEAM TAPE	SILICONE	96 Hours Salt Atmosphere	0/25
				plus	
				48 Hours Pressure Cooker (30 PSIA, 121°C)	0/24
				plus	
				1008 Hours 85°C/85% RF Bias Life	1/23 (1)
CA741G	PLASMA Si_3N_4	BEAM TAPE	SILICONE	48 Hours Salt Atmosphere (Method 1009.1)	0/12
				TEST COMPLETE	
				plus	
				1512 Hours 85°C/85% RH Bias Life	0/12
CA741G	PLASMA Si_3N_4	BEAM TAPE	SILICONE	96 Hours Salt Atmosphere (Method 1009.1)	0/43
				plus	
				GP 1: 85°C/85% RH Bias Life 1000 Hr.	1/12 (2)
				GP 2: 250°C Bias Life	In Progress
				GP 3: Pressure Cooker 48 Hrs.	0/14

(1) 1 Unit lost due to lead corrosion after pressure cooker. 1 Unit cracked after 163 hrs. of 85°C/85% RH Bias humidity life test

(2) 1 Unit cracked open after 1000 hours 85°C/85% RH bias/humidity

Fig. IV-2

Step Stress Matrix CA741 and CD4012D

The initial results of reliability testing for Phase II are summarized in Tables I through VII and the data tabulated in Tables VIII through XIV. These tables provide the unit number of verified failures and the cumulative failures at down periods for the units. Comments concerning specific unit failures in the tabulated data (Tables VIII through XIV) are provided with each table.

An analysis summary of the storage life data is presented in Tables I through VII. There was no significant difference among levels of main effects at this time in plastic devices. Preliminary failure analysis of the catastrophic (opens and shorts) units in the unlidded (open) ceramic package have shown handling damage (mainly) which is not unexpected where pellet and bondwires are exposed.

An analysis summary of the bias life data is presented in Tables VIII through XIV. While it is too early in the evaluation to draw conclusions, the number of failures was not considered excessive for unscreened devices tested to the tight MIL-M-38510 detail sheet. More hours on testing are required to determine if these failures are screenable. There was no significant difference among levels of main effects at this time in the plastic devices.

The data, as expected, show lower failures for storage life than comparable bias life for the CD4012 device.

Baseline Costs for Commercial High Reliability Plastic Product

A flow chart defining commercial high reliability DIP integrated circuits at RCA is shown in Fig. IV-3. A normalized cost matrix for this type of product assembled off-shore and domestically is shown below:

	Std DIP	Commercial Hi Rel DIP
Offshore	1.0	1.45
Domestic	3.07	4.78

TABLE I
STRESS TEST DATA SUMMARY

TEST: Storage Life

TEMPERATURE: 150°C

DURATION: 168 Hours

TYPE: CA741

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	0/15	0/15	0/15		
WIRE BOND	0/15	0/15	0/15	0/15	0/15

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE II
STRESS TEST DATA SUMMARY

TEST: Storage Life

TEMPERATURE: 175°C

DURATION: 168 Hours

TYPE: CA741

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	1/15	0/15	0/15		
WIRE BOND	0/15	0/15	0/15	0/15	0/15

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE III
STRESS TEST DATA SUMMARY

TEST: Storage Life

TEMPERATURE: 150°C

DURATION: 24 Hours

TYPE: CD4012

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	0/15	0/15	0/15		
WIRE BOND	0/15	0/15	0/15	0/15	1/15

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE IV
STRESS TEST DATA SUMMARY

TEST: Storage Life

TEMPERATURE: 175°C

DURATION: 24 Hours

TYPE: CD4012

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	0/15	0/15	0/15		
WIRE BOND	0/15	0/15	1/15	0/15	0/15

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE V
STRESS TEST DATA SUMMARY

TEST: Storage Life

TEMPERATURE: 200°C

DURATION: 16 Hours

TYPE: CD4012

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	0/15	0/15	0/15		
WIRE BOND	0/15	0/15	1/15	1/15	3/15

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE VI
STRESS TEST DATA SUMMARY

TEST: Bias Life

TEMPERATURE: 150°C

DURATION: 26 Hours

TYPE: CD4012

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	1/20	4/20	1/20		
WIRE BOND	2/20	2/20	3/20	3/10	1/10

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE VII
STRESS TEST DATA SUMMARY

TEST: Bias Life

TEMPERATURE: 175°C

DURATION: 24 Hours

TYPE: CD4012

	PLASTIC			CERAMIC	
	SILICONE	2930	2930 + JC	SEALED	OPEN
BEAM TAPE	0/14	1/14	4/14		
WIRE BOND	1/14	3/14	0/14	1/10	2/10

X/Y

X = NUMBER OF VERIFIED FAILURES
Y = TOTAL DEVICES ON TEST

TABLE VIII

BEAM TAPE — WIRE BOND — 150°C Storage CA741

CELL	1	2	3	4	5	6	7	8	
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN	COMMENTS
QTY / HR	15	15	15	15	15	15	15	15	
8	0	0	0	0	0	0	0	0	
24	0	0	0	0	0	0	0	0	
168	0	0	0	0	0	0	0	0	

TABLE IX

BEAM TAPE → | WIRE BOND →

175°C Storage
CA741

CELL	1	2	3	4	5	6	7	8	
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN	COMMENTS
QTY / HR	15	15	15	15	15	15	15	15	
8	0	0	0	0	0	0	0	0	#25-1 Open
24	0	0	0	0	0	0	0	0	
168	#25 1	0	0	0	0	0	0	0	

TABLE X

150°C Storage Life
CD4012

BEAM TAPE → WIRE BOND →

CELL	1	2	3	4	5	6	7	8		
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN	COMMENTS	
QTY / HR	15	15	15	15	15	15	15	15		
8	0	0	0	0	0	0	0	0	#90-8	Open
24	0	0	0	0	0	0	0	#90 1		

TABLE XI

BEAM TAPE ← → WIRE BOND

175°C Storage Life

CD4012

CELL	1	2	3	4	5	6	7	8	
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN	COMMENTS
QTY / HR	15	15	15	15	15	15	15	15	
8	0	0	0	0	0	0	#16 1	0	#16-8 Leakage
24	0	0	0	0	0	0	1	0	

TABLE XII

200°C Storage Life
CD4012

	BEAM TAPE			WIRE BOND				
CELL	1	2	3	4	5	6	7	8
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN
QTY / HR	15	15	15	15	15	15	15	15
2	0	0	0	0	0	0	#35 1	#45 1
4	0	0	0	0	0	0	1	#49 2
8	0	0	0	#34 1	0	0	1	2
16	0	0	0	1	0	0	1	#41 3
32	0	#36 1	0	#31 2	0	0	1	3

COMMENTS

#45-8, #41-8 Open
#49-8 Short
#34-4 LKG (MARG @ 8 HR, Worse @ 16 HR)
#35-7 Leakage
#36-2 Leakage

TABLE XIII

150°C Bias Life
CD4012

	BEAM TAPE			WIRE BOND				
CELL	1	2	3	4	5	6	7	8
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN
QTY / HR	20	20	20	10	20	20	20	10
8	#86 1	#90,91, 92,95 4	#80 1	#7 1	#29 1	#81 1	#80,86 87 3	0
26	1	4	1	#1,4 3	#93 2	#17 2	3	#10 1

COMMENTS

#86-1, 42-2, 80-5, 81-6, 1-4, 4-4, 79-5, 86-7, 87-7 Leakage (Marginal)
#91-2, 95-2, 90-2 Leakage
#7-4 Output Voltage (Marginal)
#93-5 Leakage & Output Voltage
#80-7 Output Voltage (Marginal)
#10-8 Multiple Fail

TABLE XIV

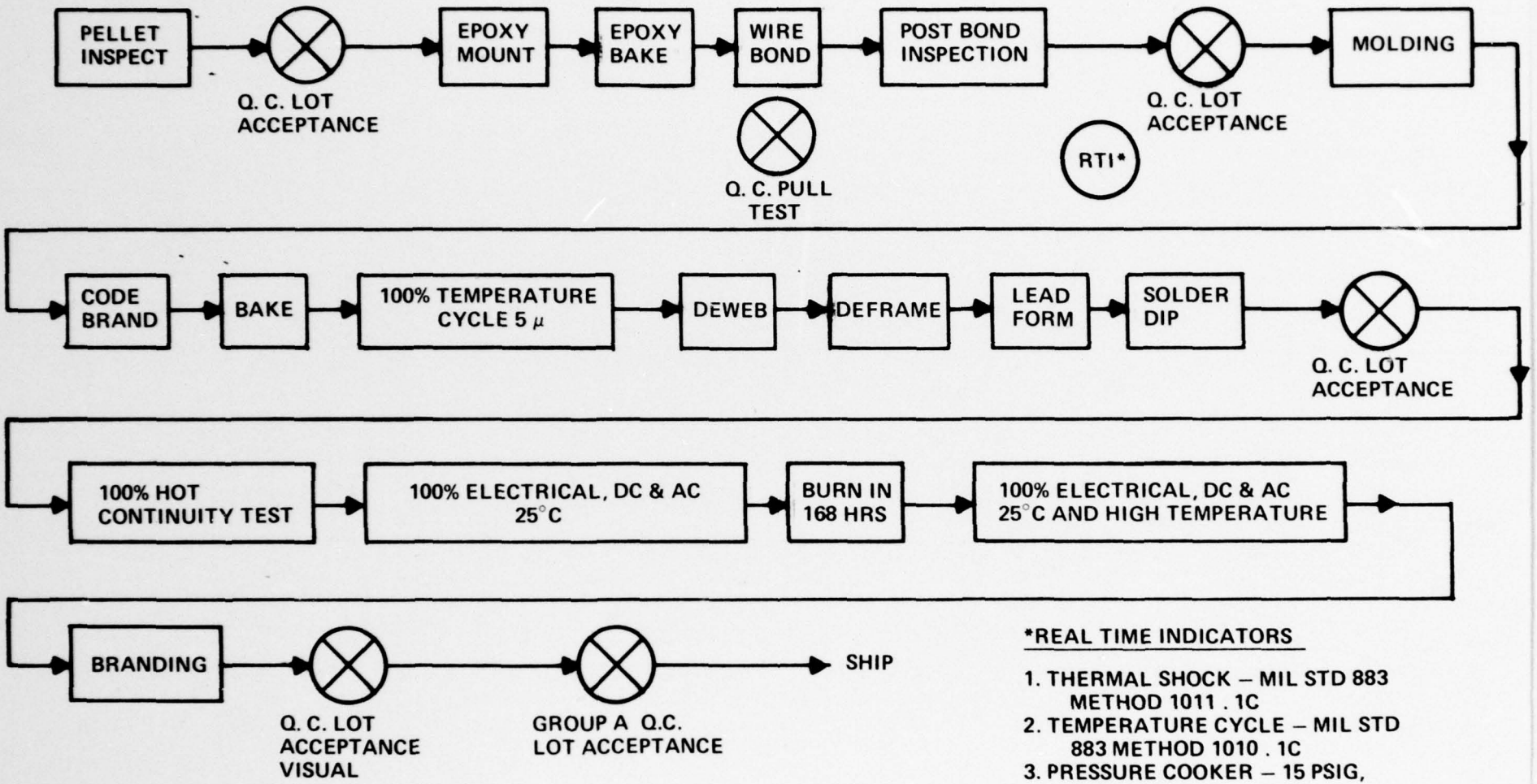
175°C Bias Life
CD4012

	BEAM TAPE			WIRE BOND				
CELL	1	2	3	4	5	6	7	8
CI	SILICONE	2930	2930 +JC	DIC SEALED	SILICONE	2930	2930 +JC	DIC OPEN
QTY / HR	14	14	14	10	14	14	14	10
8	0	#104 1	#107 1	#18 1	#103 1	0	0	#13 1
24	0	1	#103,105, 109 4	1	1	#116,104, 107 3	0	#14 2

COMMENTS

#104-2, 116-6, 104-6, 108-6 Leakage
#107-3 Leakage (Marginal)
#18-4 Output Voltage (Marginal)
#103-5 Output Voltage
#103-3, 105-3, 109-3, 14-8 Leakage & Output Voltage
#13-8 Leakage & Output Voltage @ 8 HR
(Open @ 16 HR)

COMMERCIAL HI-REL FLOW CHART



*REAL TIME INDICATORS

1. THERMAL SHOCK – MIL STD 883 METHOD 1011 . 1C
2. TEMPERATURE CYCLE – MIL STD 883 METHOD 1010 . 1C
3. PRESSURE COOKER – 15 PSIG, 96 HOURS

Fig. IV-3

SECTION V

TECHNICAL PRESENTATIONS RELATED TO HRLC TECHNOLOGY

Oct 4, 1977, U.S. Army Electronics Command, Fort Monmouth, N.J. A.S. Rose.

Oct. 14, 1977, Lockheed Missile & Space Corporation, Sunnyvale, California, A.S. Rose.

SECTION VI
CONCLUSIONS

1. Wafer fabrication for Phase II is nearing completion.

2. Reliability of the copper beam-epoxy molding compound system has proven unsatisfactory.

3. The reliability of the silicone molding compound has been excellent with respect to electrical parameters, sequential salt atmosphere and moisture testing. This compound has met the requirements for high reliability low-cost integrated circuits and will be used in the assembly of final Phase II product.

SECTION VII

PLANS FOR THE NEXT INTERVAL

1. Complete assembly and test of the required circuits.
2. Continue reliability testing.
3. Delivery of final samples of all integrated circuit types.

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